



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/789,443	02/27/2004	Promod Kumar	01CT33753406	4859
27975	7590	06/17/2005		EXAMINER
				LUU, PHO M
			ART UNIT	PAPER NUMBER
				2824

DATE MAILED: 06/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/789,443	KUMAR ET AL.	
	Examiner Pho M. Luu	Art Unit 2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on \_\_\_\_\_.
- 2a) This action is FINAL.                            2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 4-16 is/are pending in the application.
  - 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) 4-10 and 13-16 is/are allowed.
- 6) Claim(s) 11 and 12 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 27 February 2004 is/are: a) accepted or b) objected to by the Examiner.
 

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    - a) All    b) Some \* c) None of:
      1. Certified copies of the priority documents have been received.
      2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
      3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | Paper No(s)/Mail Date. _____.   |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>11/08/04</u> . | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
|   | 6) <input checked="" type="checkbox"/> Other: <u>Search History</u> .       |

**DETAILED ACTION**

1. Acknowledgment is made of applicant's Preliminary Amendment filed 27 February 2004. The changes and remarks disclosed therein were considered.
2. Claims 1-3 have been canceled.
3. Claims 4-16 are pending in the application.
4. This office acknowledges receipt of the following items from the Applicant:  
Declaration filed on 01 June 2004.

***Priority***

5. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

***Information Disclosure Statement***

6. Acknowledgment is made of applicant's Information Disclosure Statement (IDS) Form PTO-1449, filed 27 February 2004. The information disclosed therein was considered.

***Specification***

7. Applicant is reminded of the proper language and format for an abstract of the disclosure. The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means"

and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

8. The abstract of the disclosure is objected to because it uses the phrase "**The architecture provides for executing**" in lines 4-5, "**The processes are executed**" in lines 7-8, "**Managing test routines**" in lines 10, "**process permits the device architecture to be**" in lines 11, and "**by purposely creating a standard**" in lines 12-13, which is implied. Correction is required. See MPEP § 608.01(b).

9. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

### **Claim Rejections - 35 USC § 102**

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. Claims 11-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Chevallier (US. 6,813,183).

For the purpose of this rejection, Chevallier in Figure 1 discloses memory controller 105 interface signals to the command execution logic 140. The module 140 controls the state machine 130 which control acts necessary for program, read and erase the flash memory cell array 138 (see column 4, lines 20-25). The control 130 operation of the integrated circuit 110 such as providing write, erase to the memory array 138 through an X-interface (145) and Y-interface (150). To be more specific, Chevallier discloses in Figure 3 the method determine the selected of flash memory cell array (138) are detect and repair operation in the integrated circuit 100 (see column 6, lines 17-22).

Regarding independent claim 11, Chevallier in Figures 1-3 discloses a memory device (100, Fig 1) comprising:

a flash memory array (flash memory integrated circuit 110 includes an memory array 138, Fig. 1, see column 4, lines 16-18);  
an associated micro-controller (105, Fig.1, see explain above) for detecting failed array cells (example, method 300 in Figure 3 for test flash array (138, Fig. 1) from integrated circuit (110, Fig. 1) which is 324 indicated that the selected flash cell has failed, see column 6, lines 26-33), storing information about the detected failed array cells (example, flash cells transistor 210A-210S in Fig. 2 storing information at the floating gate, see column 5, lines 62-64) and storing the column address of column with detected failed array cells (example, bit lines BL0-BLM, Fig. 2 such as column address) (also; see column 6, lines 7-55).

With respect to dependent claim 12, Chevallier in Figures 1-3 disclosed a repair data unit associated with the microcontroller (see Figure 3, column 6, lines 17-18).

***Allowable Subject Matter***

12. Claims 4-10 and 13-16 are allowed.

The following is an examiner's statement of reasons for allowance:

There is no teaching or suggestion in the prior art to: "a circuit block including a register to store a redundancy vector to be programmed in the re-routing cams and the selected paths for programming information during execution of a cam programming process" as claimed in the independent claim 4; or

"a data comparison circuit for comparing the generated expected data with data read from a certain memory location pre-programmed with expected data" as claimed in the independent claim 7; or

"a cache address generator for generating a current address of the second cache memory based upon a current address in the address counter and the up/down counter" as claimed in the independent claim 13.

***Conclusion***

13. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Pho M. Luu whose telephone number is 571.272.1876. Examiner can normally be reached on M-F 8:00AM – 5:00PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's Supervisor, Richard Elms, can be reached on 571.272.1869. The official fax number for the organization where this application or proceeding is assigned is 703.872.9306 for all official communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see

<http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

pL

PML  
April 28 2005